

FIG. 1

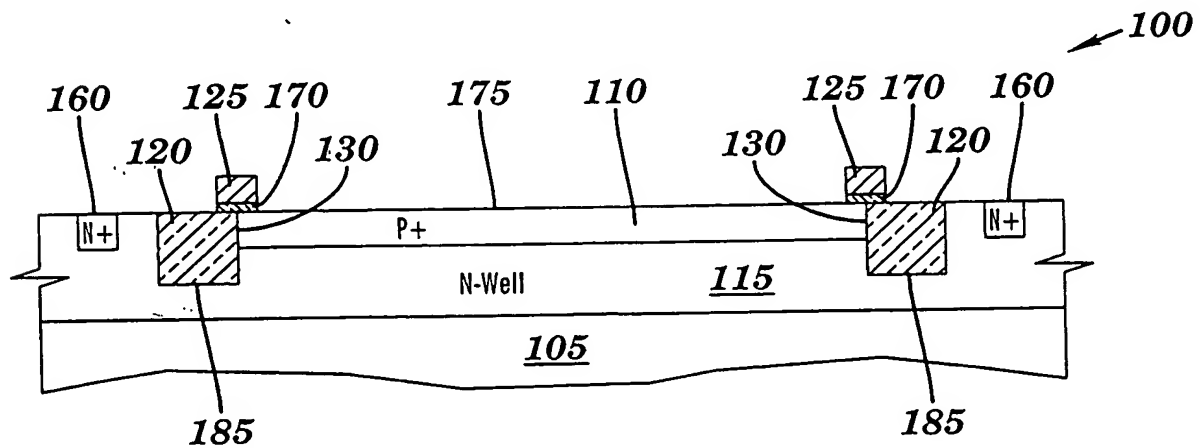


FIG. 2

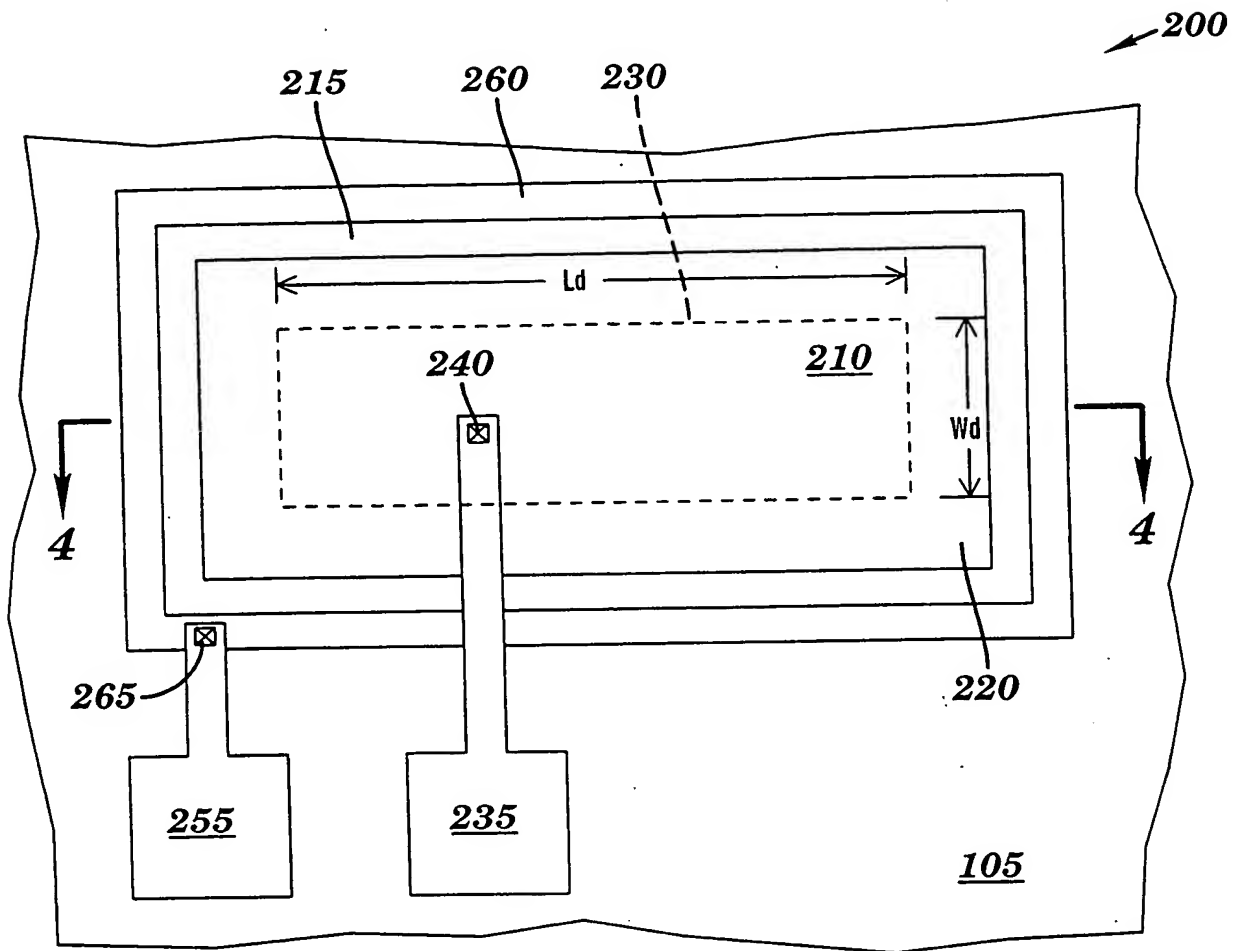


FIG. 3

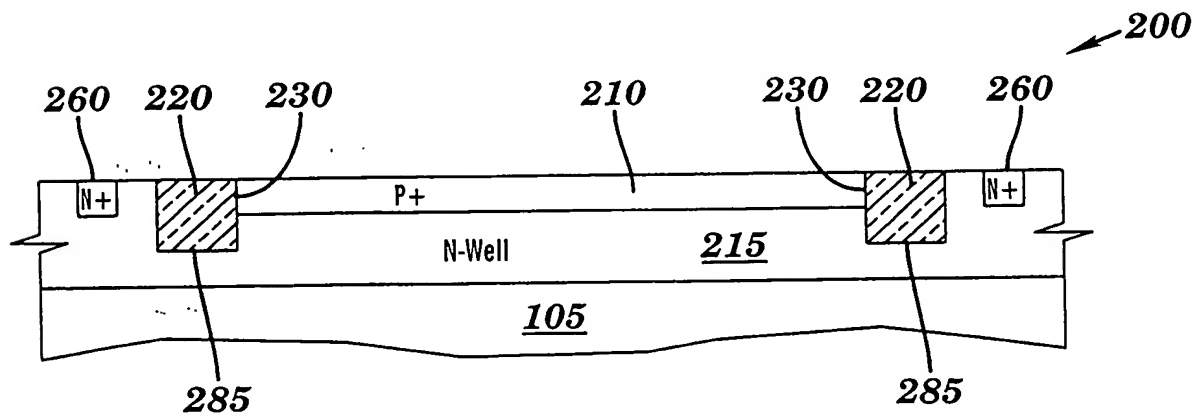


FIG. 4

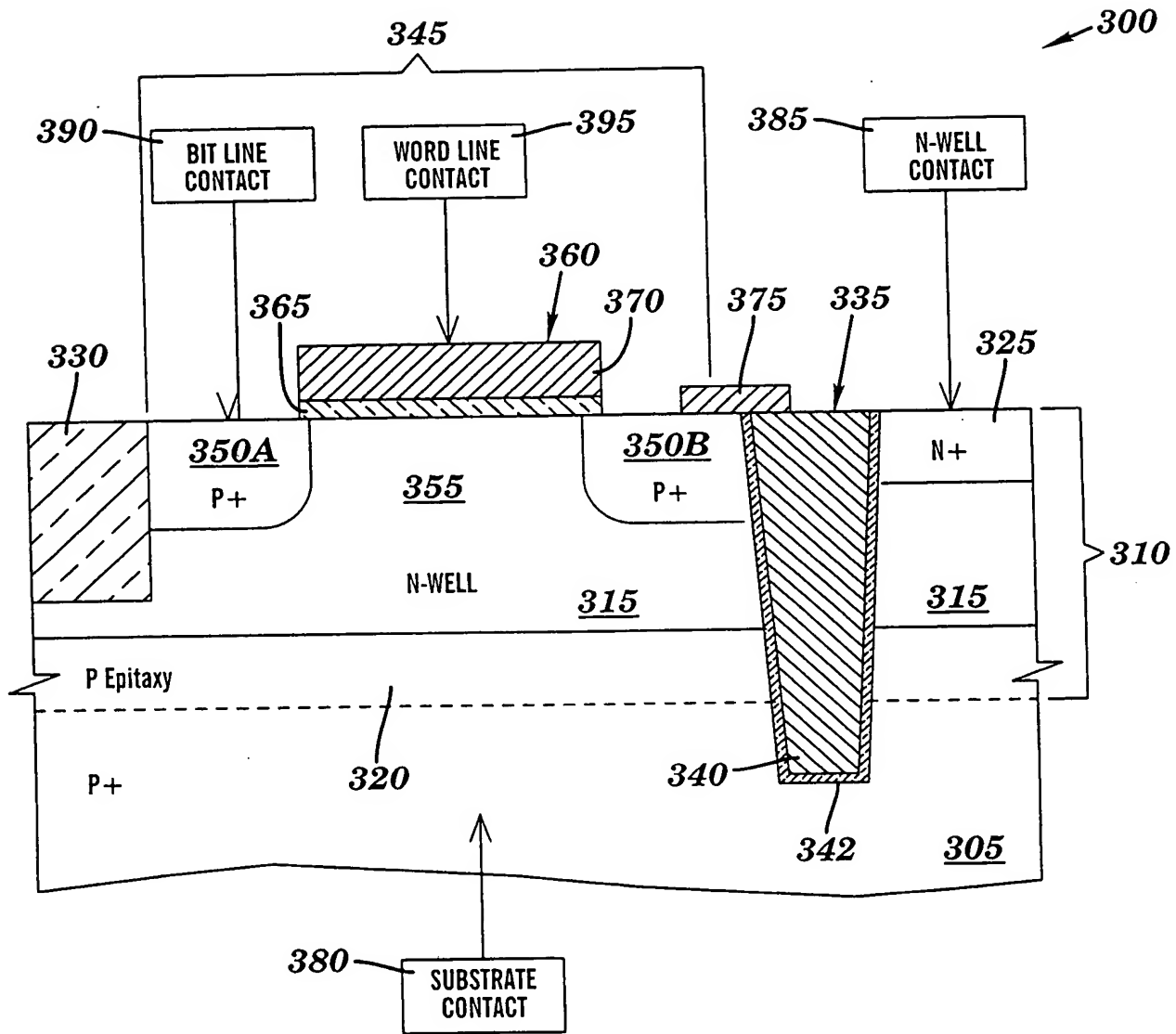


FIG. 5

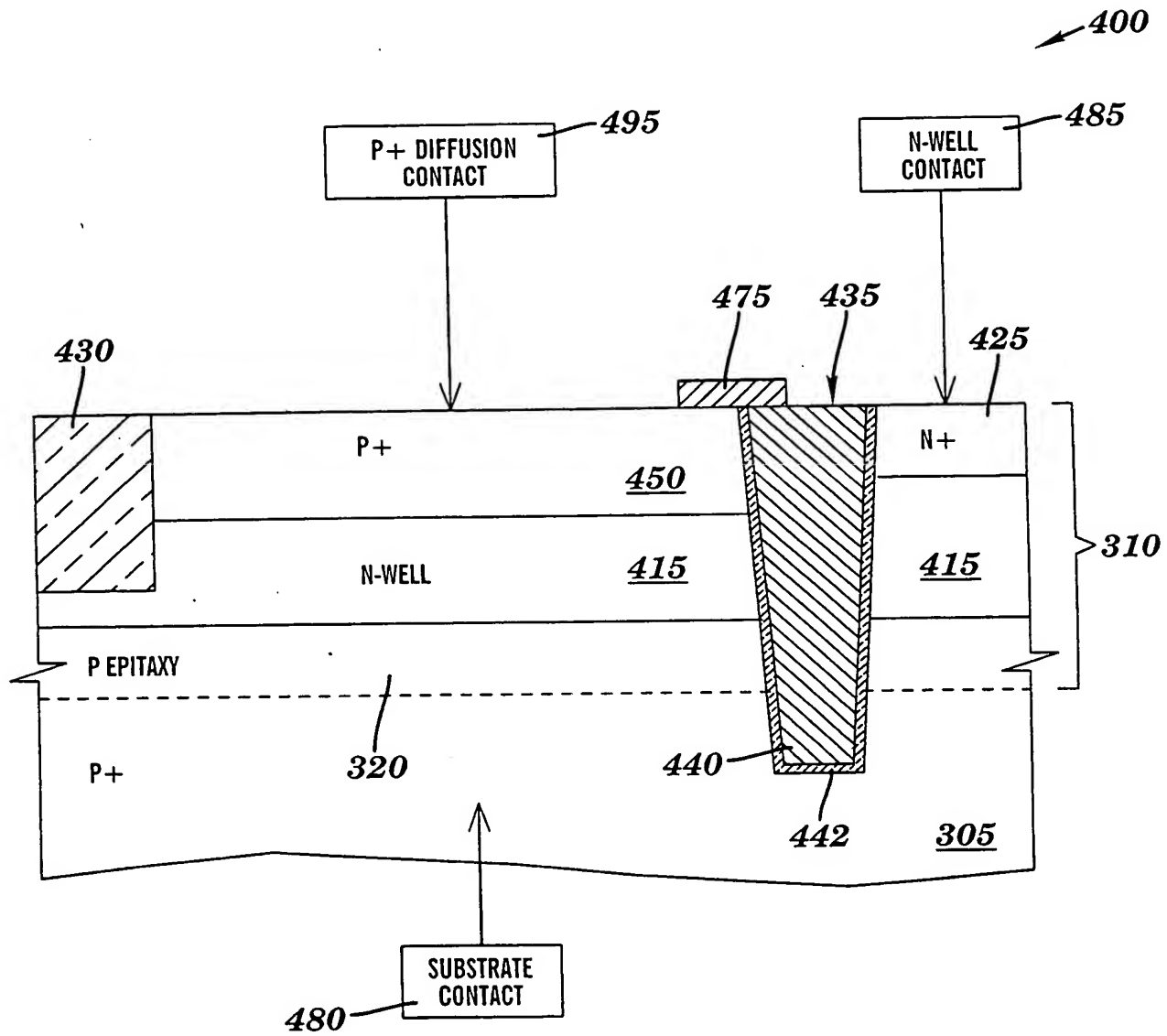


FIG. 6

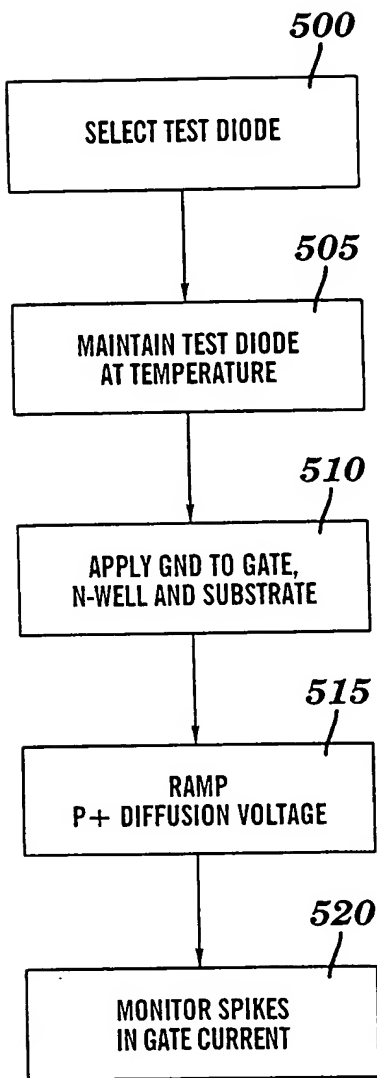


FIG. 7A

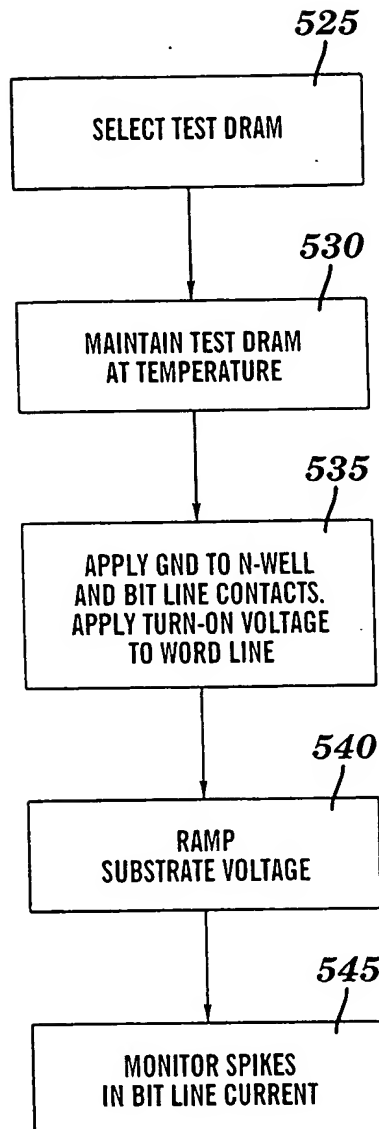


FIG. 7B

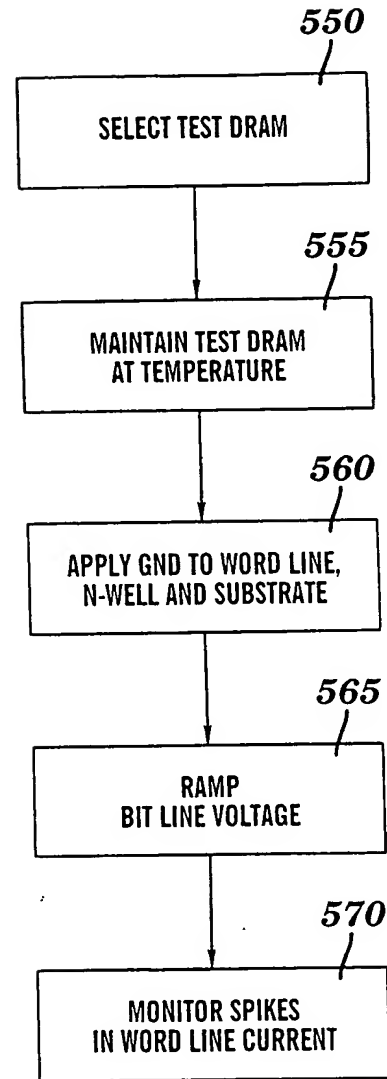


FIG. 7C

P+ POLYSILICON-BOUNDED DIODE WITHOUT STRESS-INDUCED DEFECTS

GATE AND DIFFUSION CURRENTS AT 180C AND 5nm THERMAL OXIDE

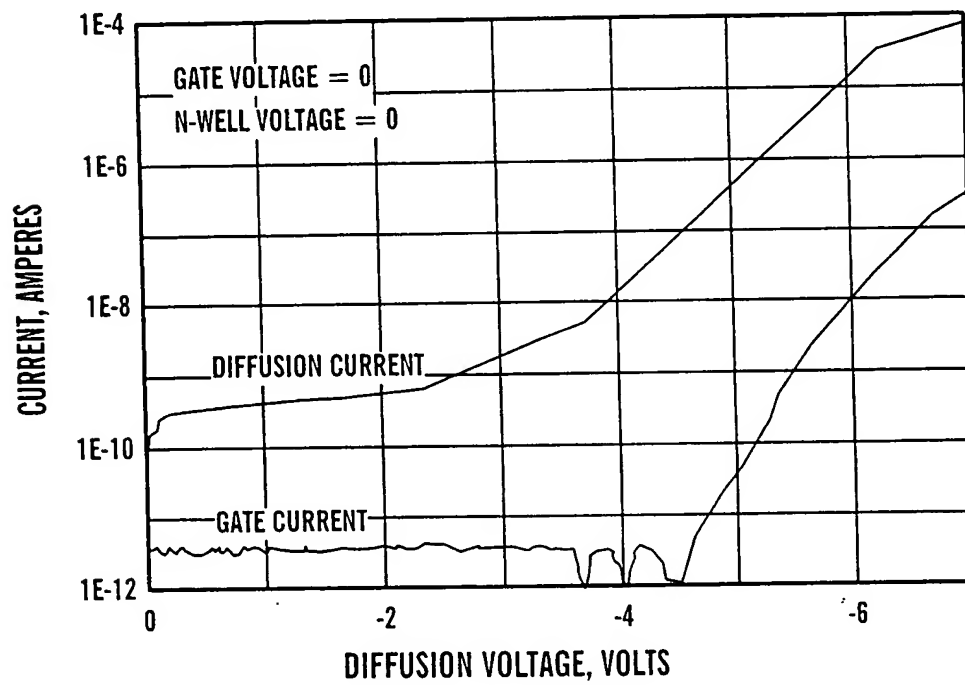


FIG. 8

P+ POLYSILICON-BOUNDED DIODE WITH STRESS-INDUCED DEFECTS

GATE AND DIFFUSION CURRENTS AT 180C AND 5nm THERMAL OXIDE

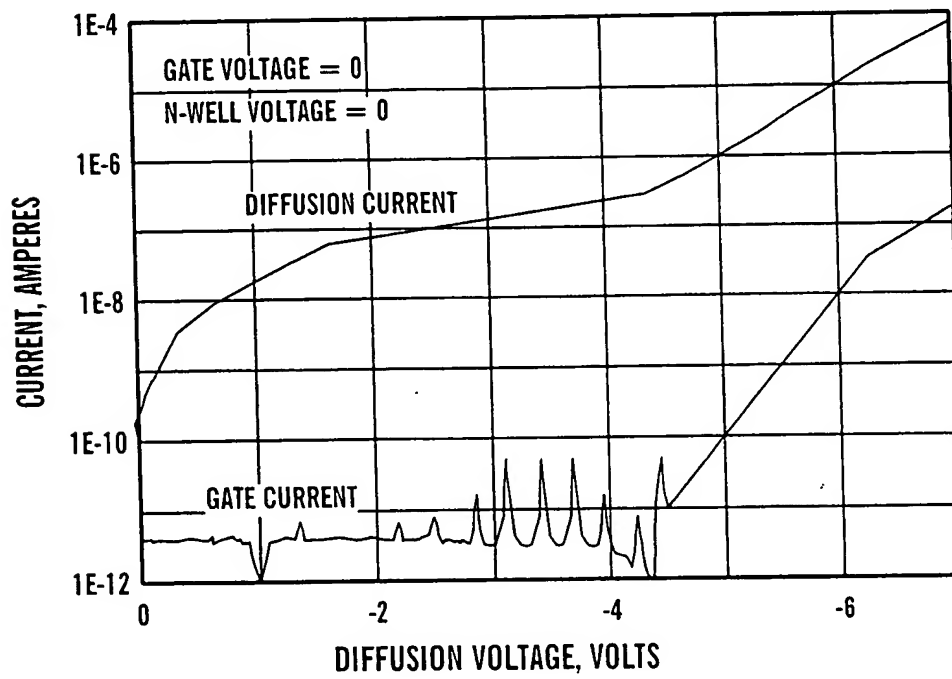


FIG. 9

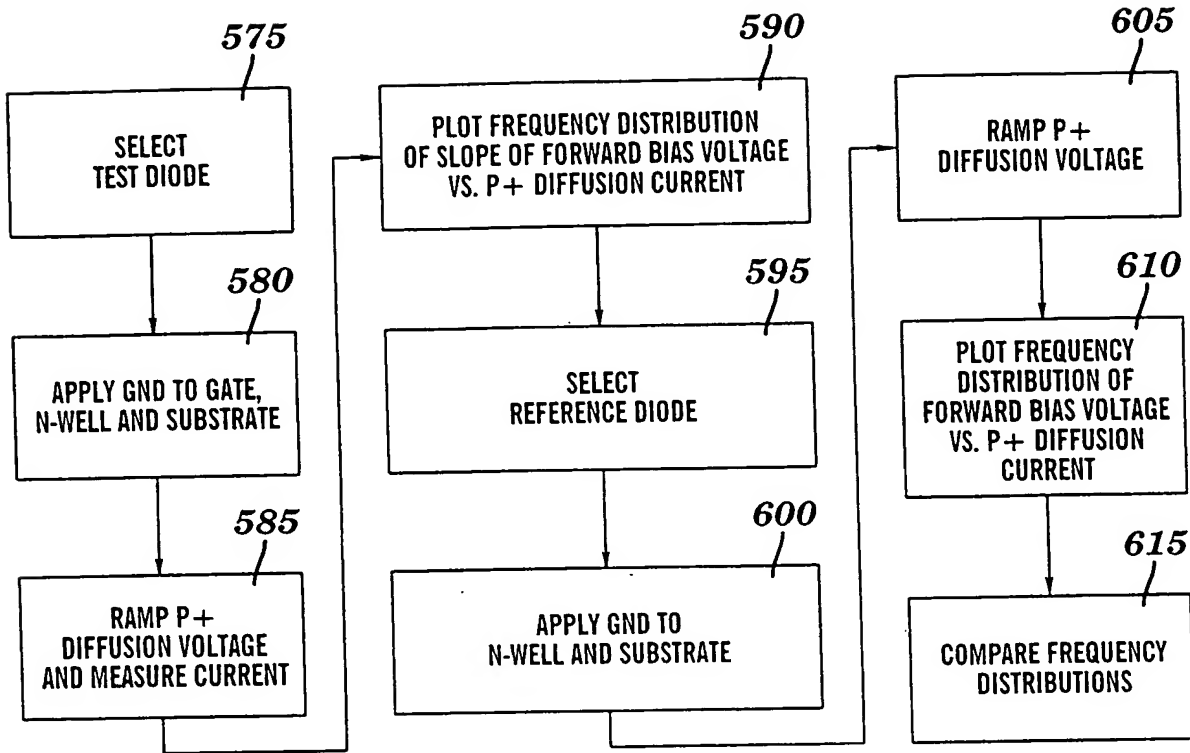


FIG. 10A

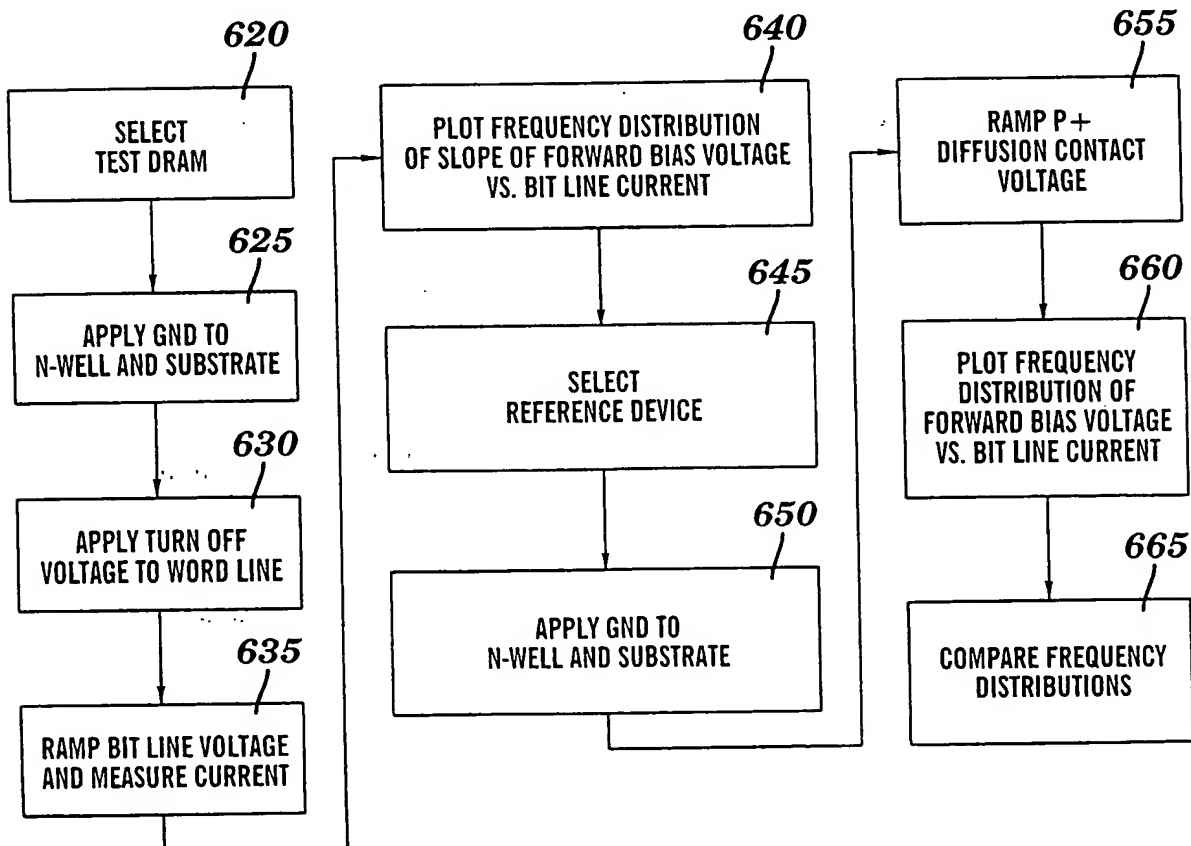


FIG. 10B

P+/N-WELL FORWARD BIASED POLYSILICON BOUNDED DIODE CURRENT VS. VOLTAGE

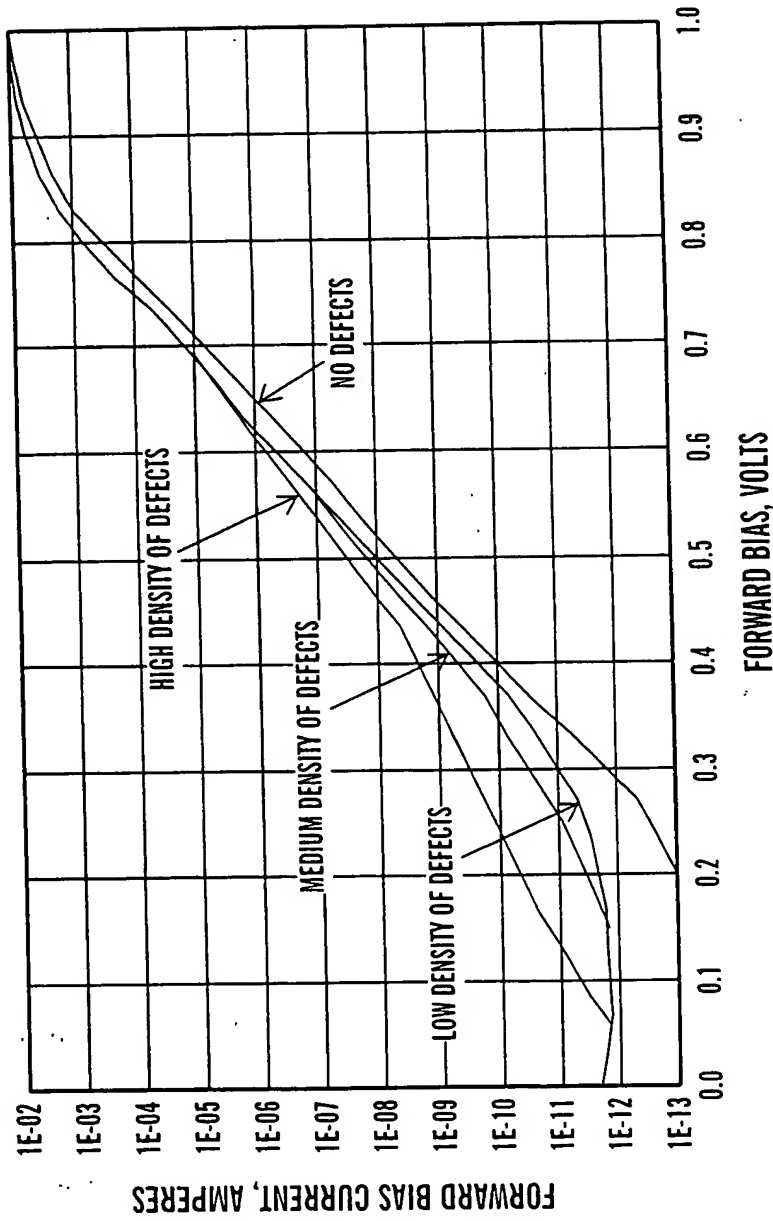


FIG. 11

FORWARD BIAS VOLTAGE VS. CURRENT SLOPE AT FORWARD BIAS VOLTAGE OF 0.45 VOLTS

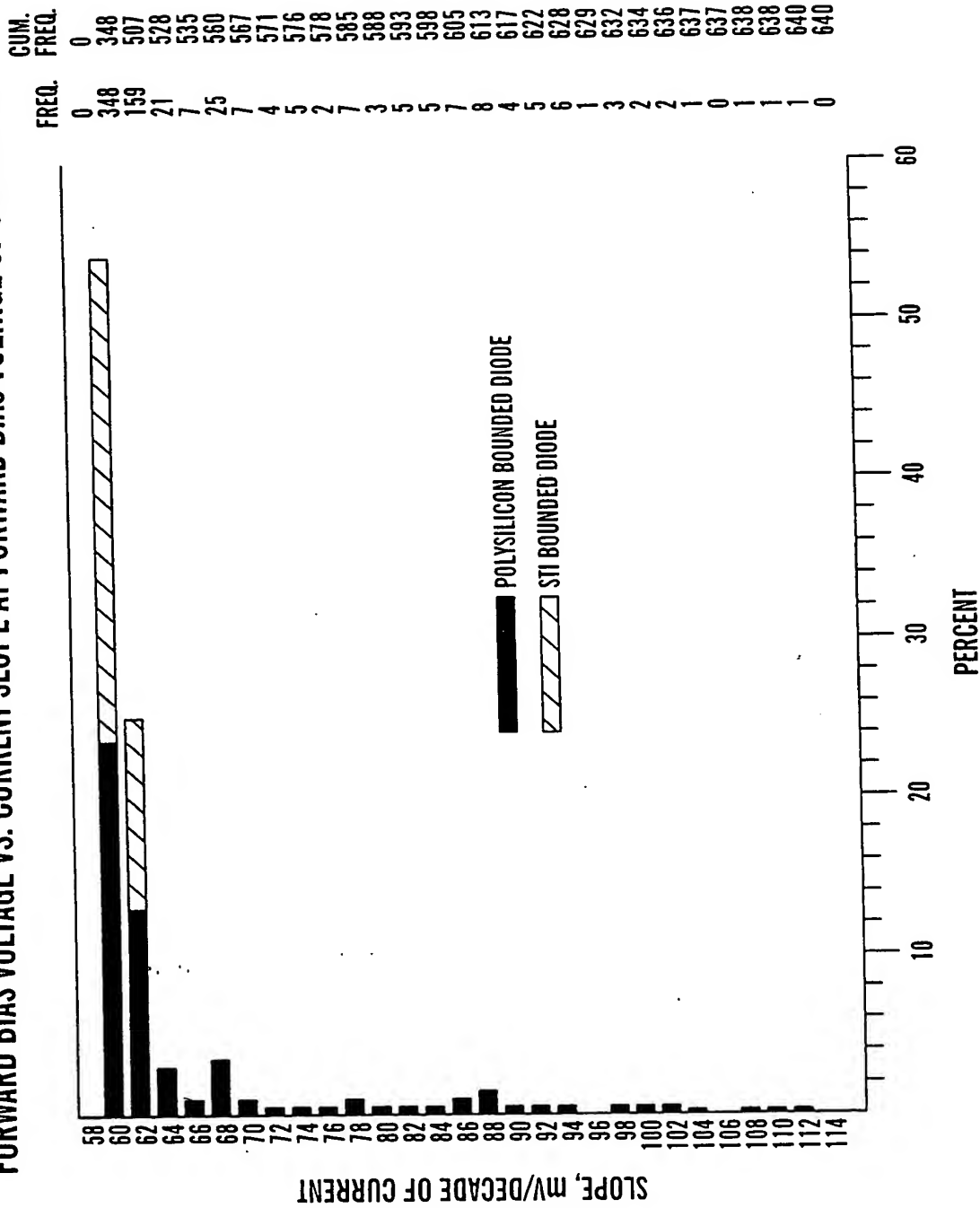


FIG. 12

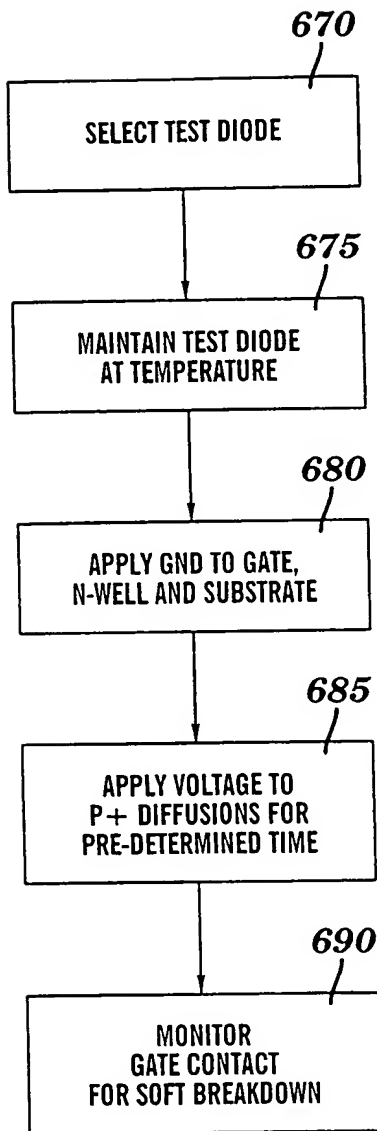


FIG. 13A

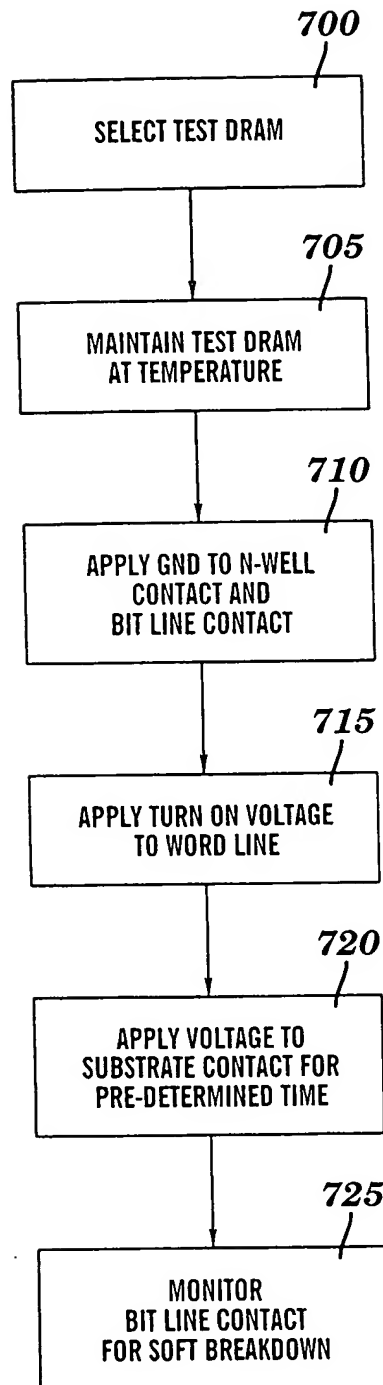


FIG. 13B

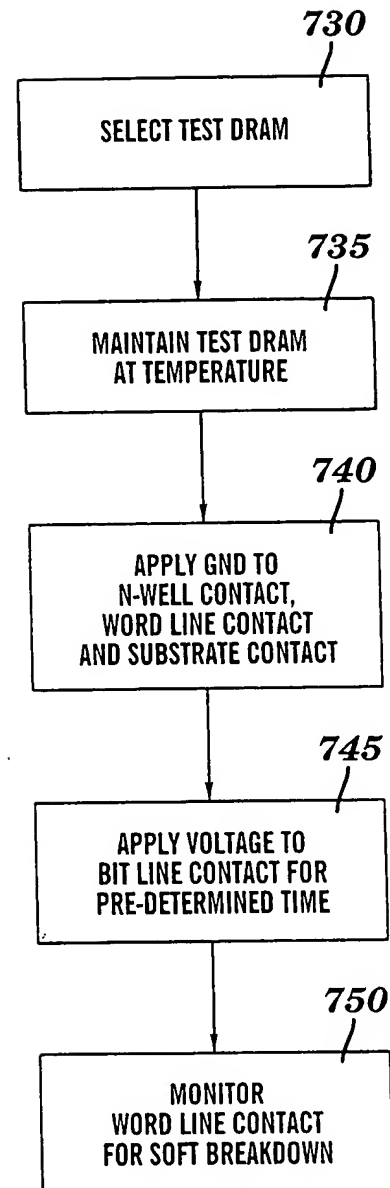


FIG. 13C

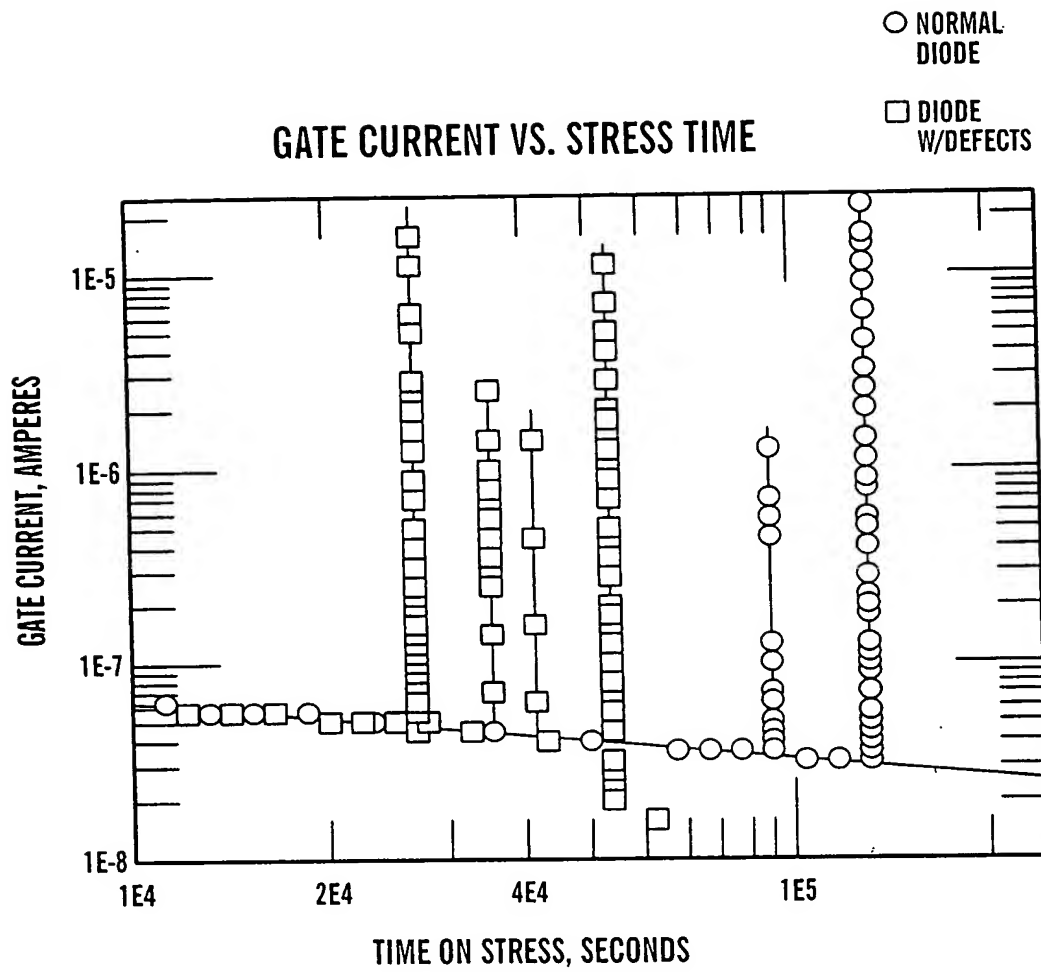


FIG. 14

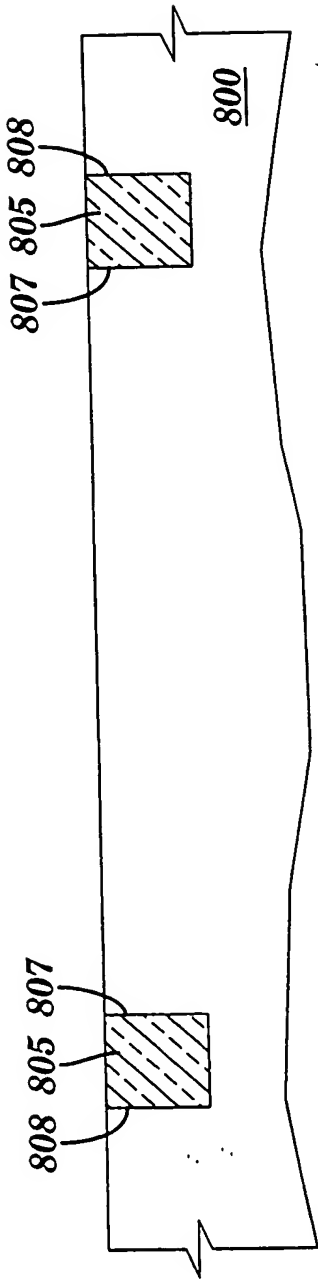


FIG. 15A

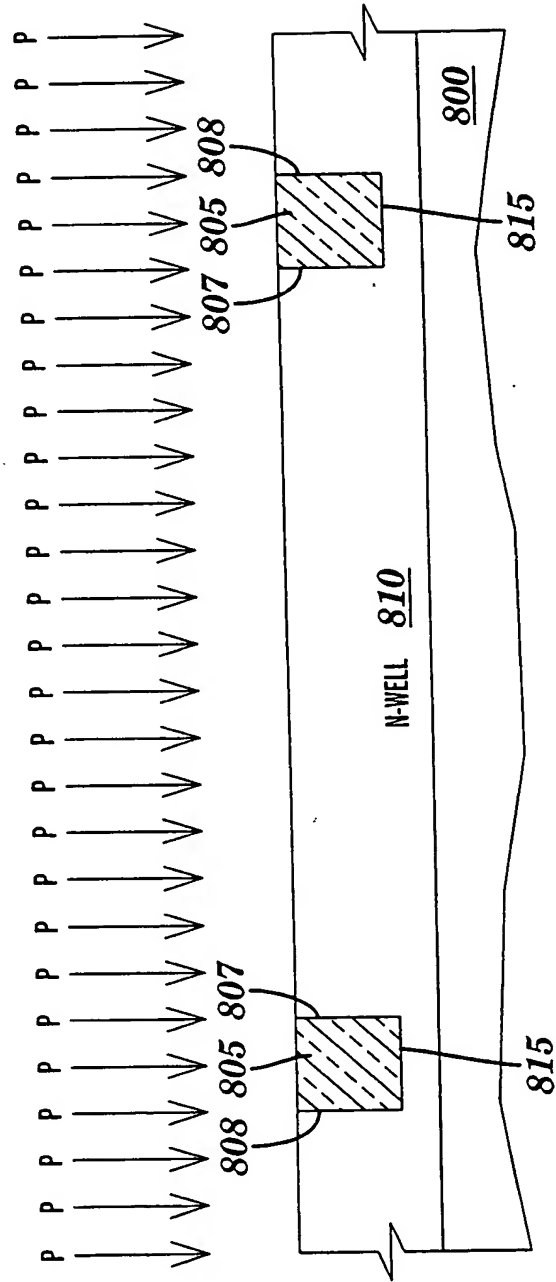


FIG. 15B

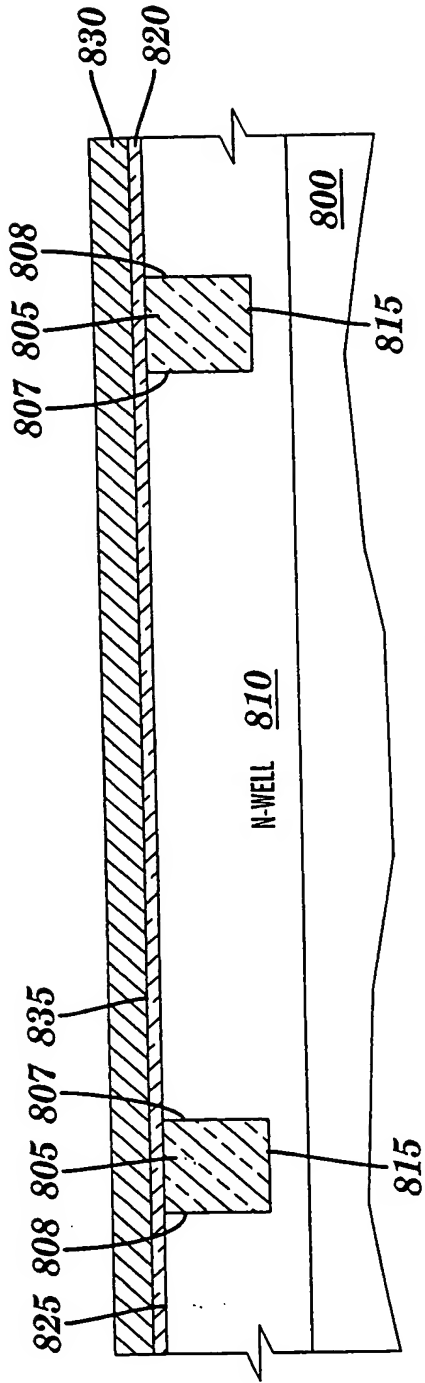


FIG. 15C

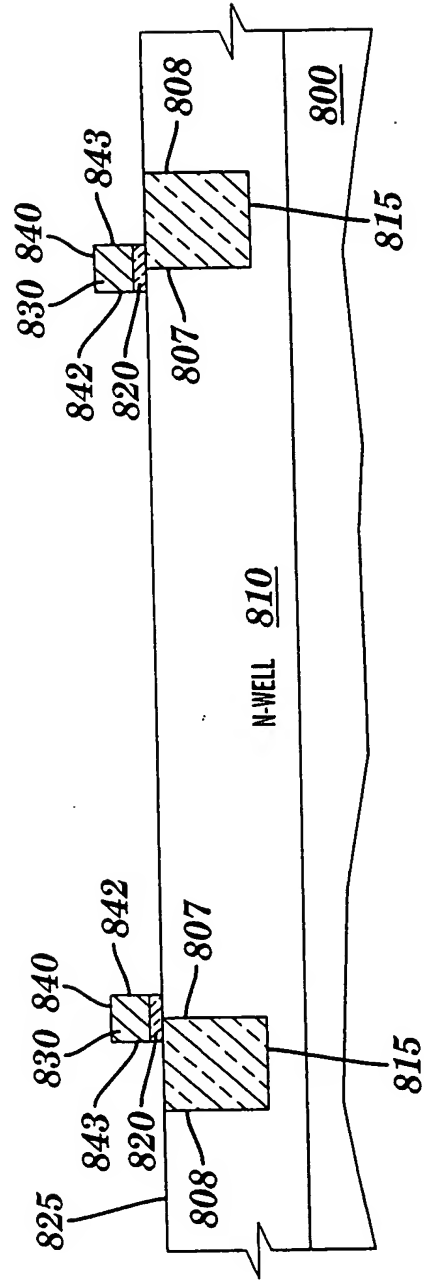
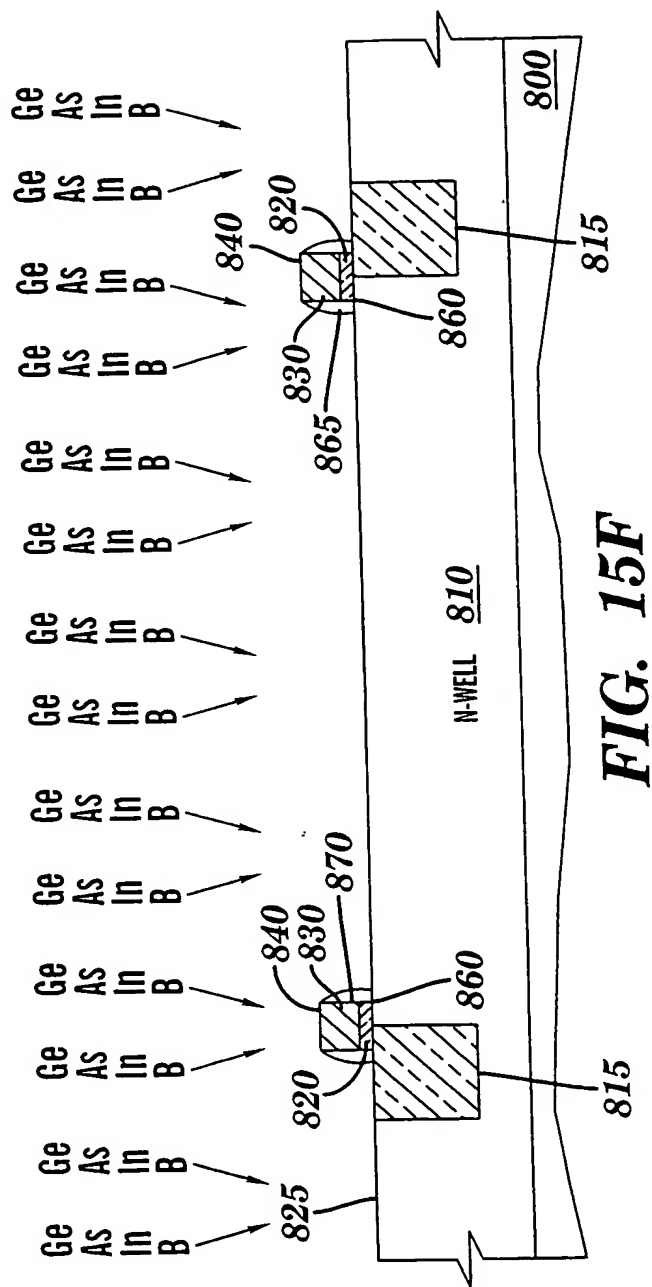
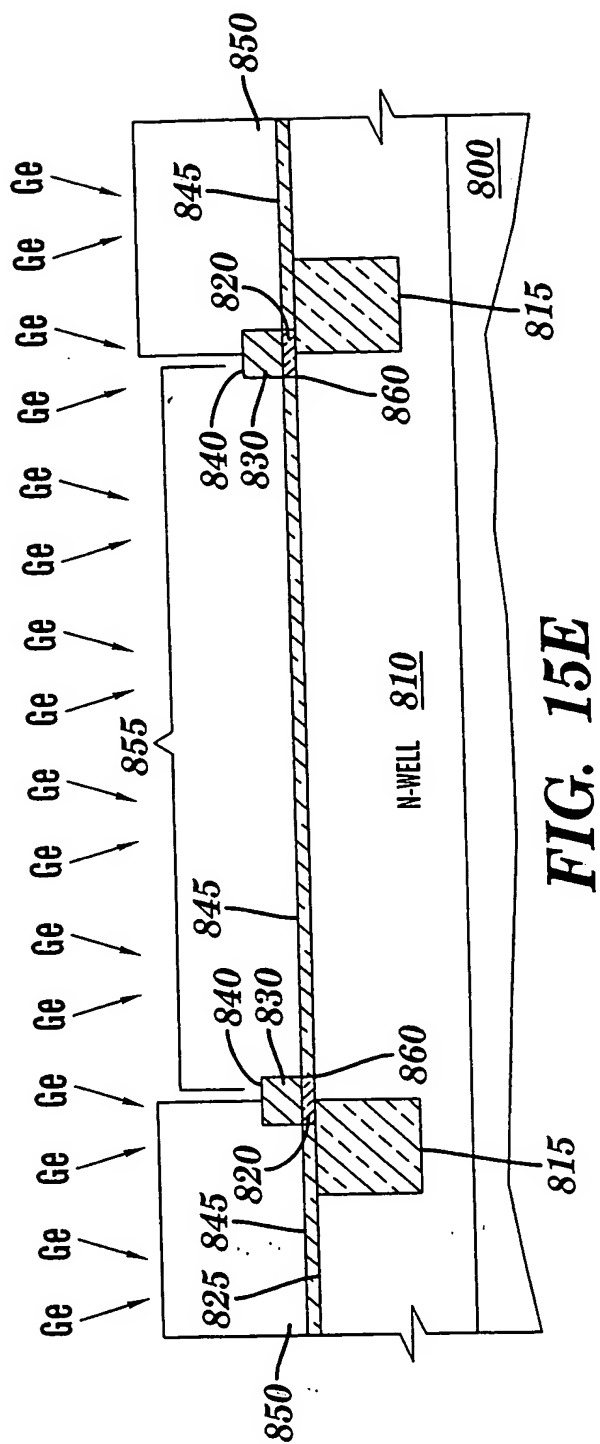


FIG. 15D



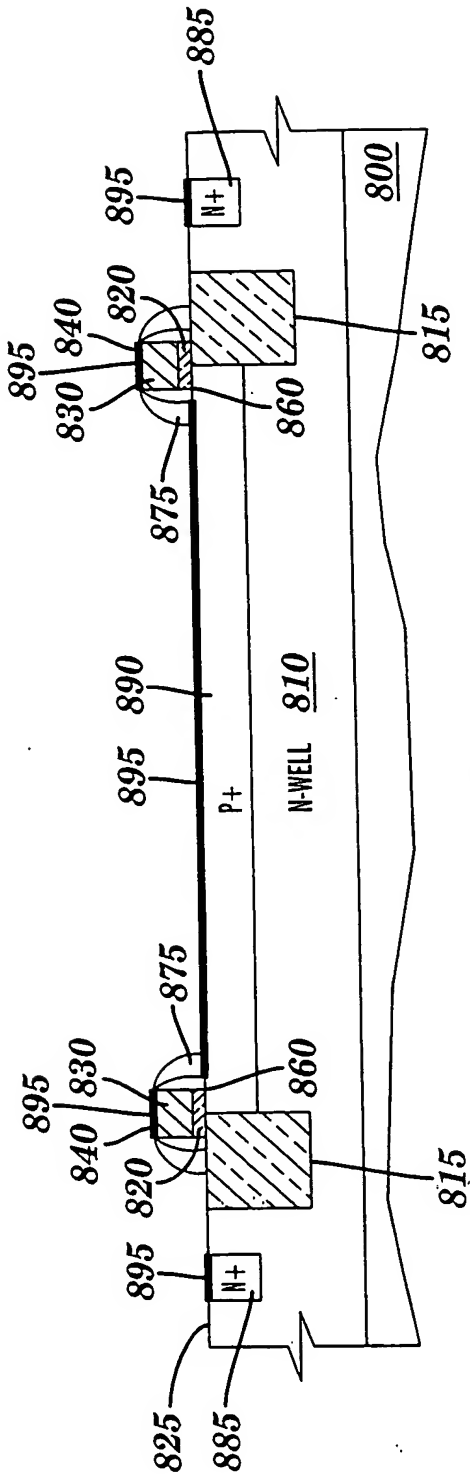


FIG. 15J

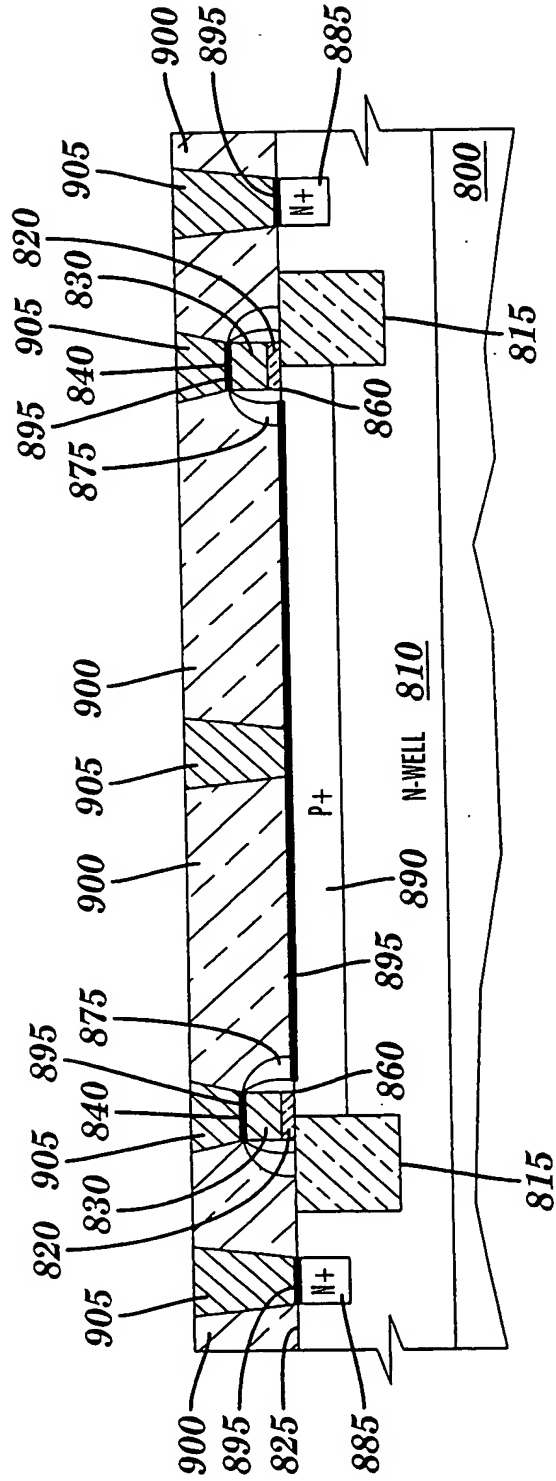


FIG. 15K

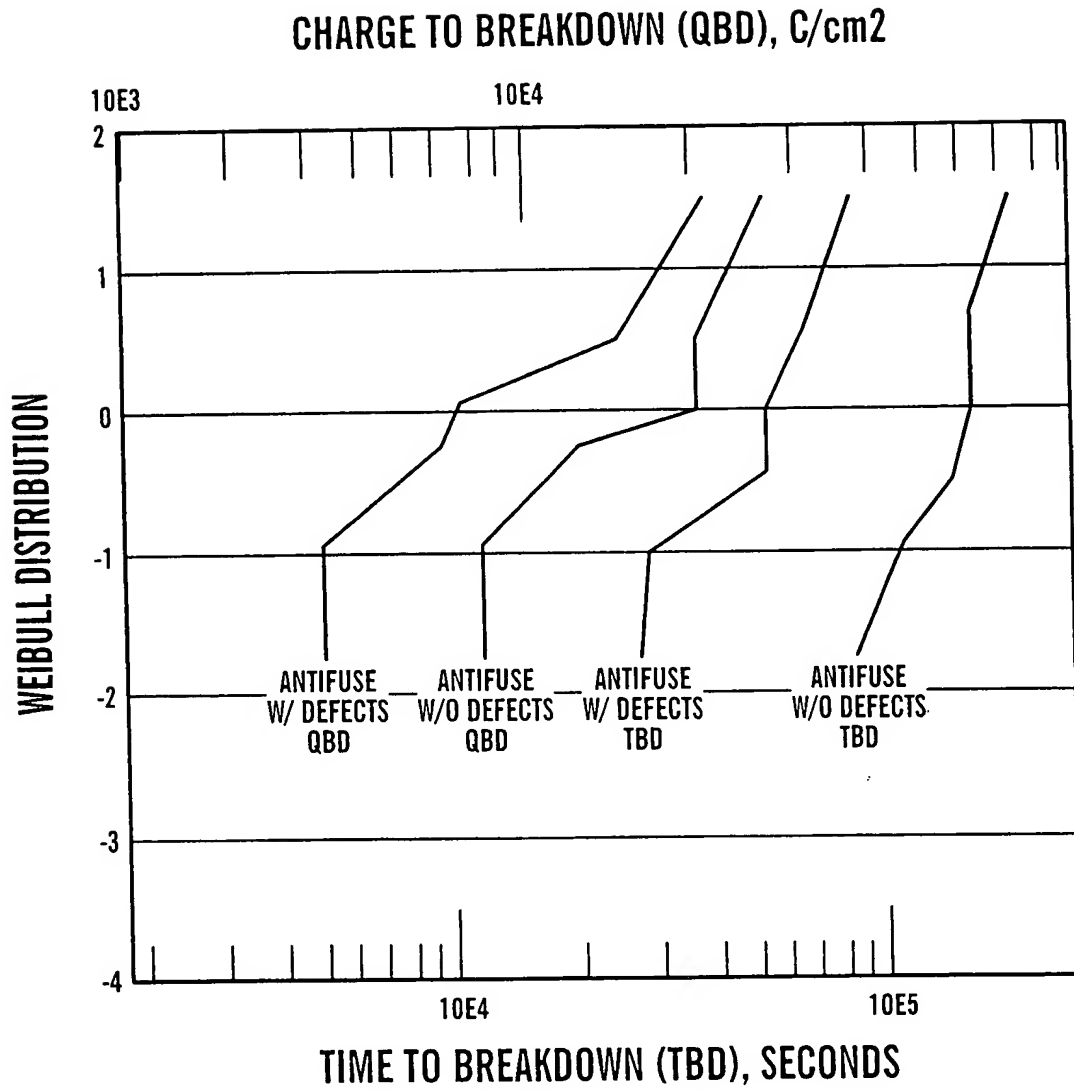


FIG. 16

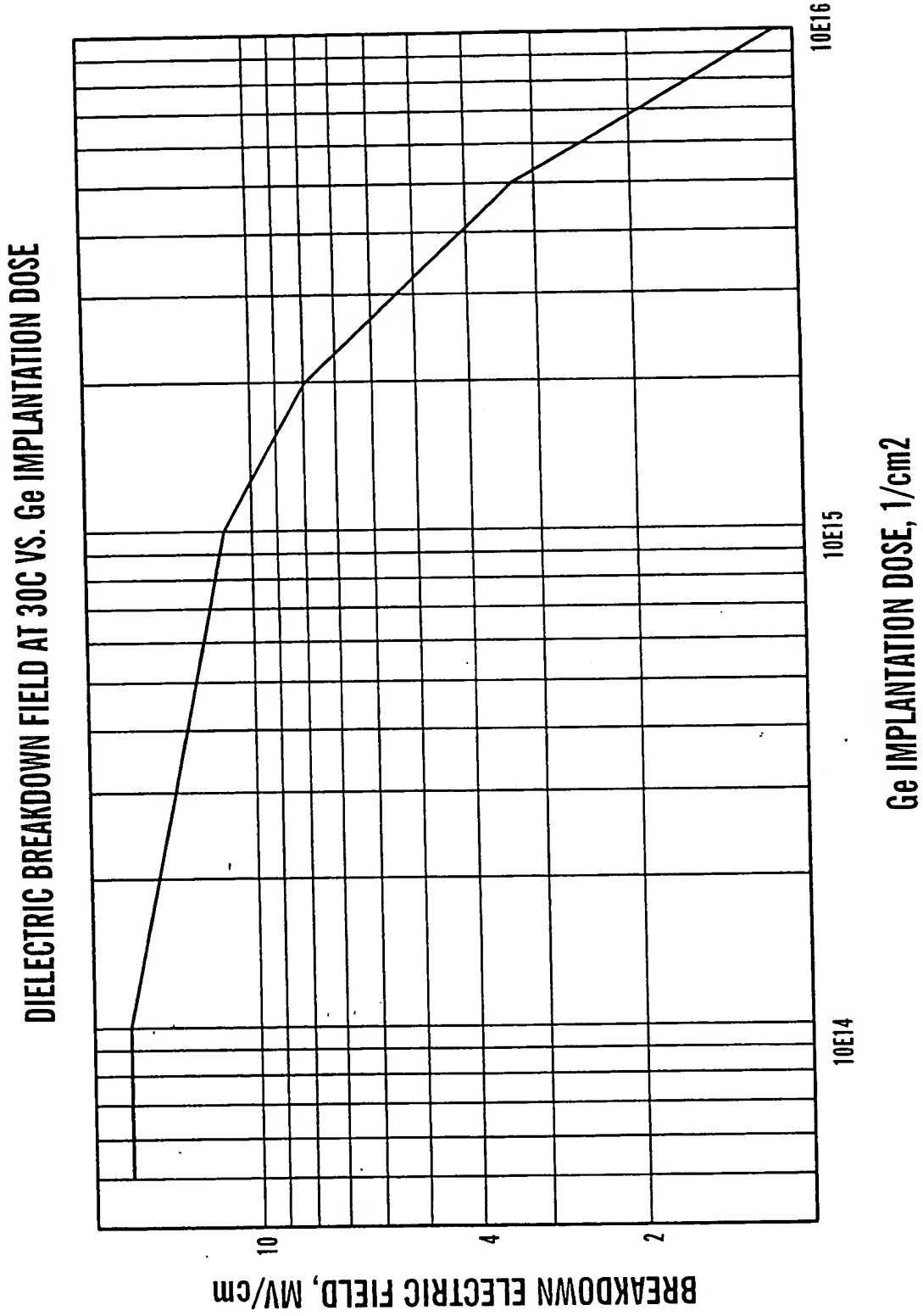


FIG. 17

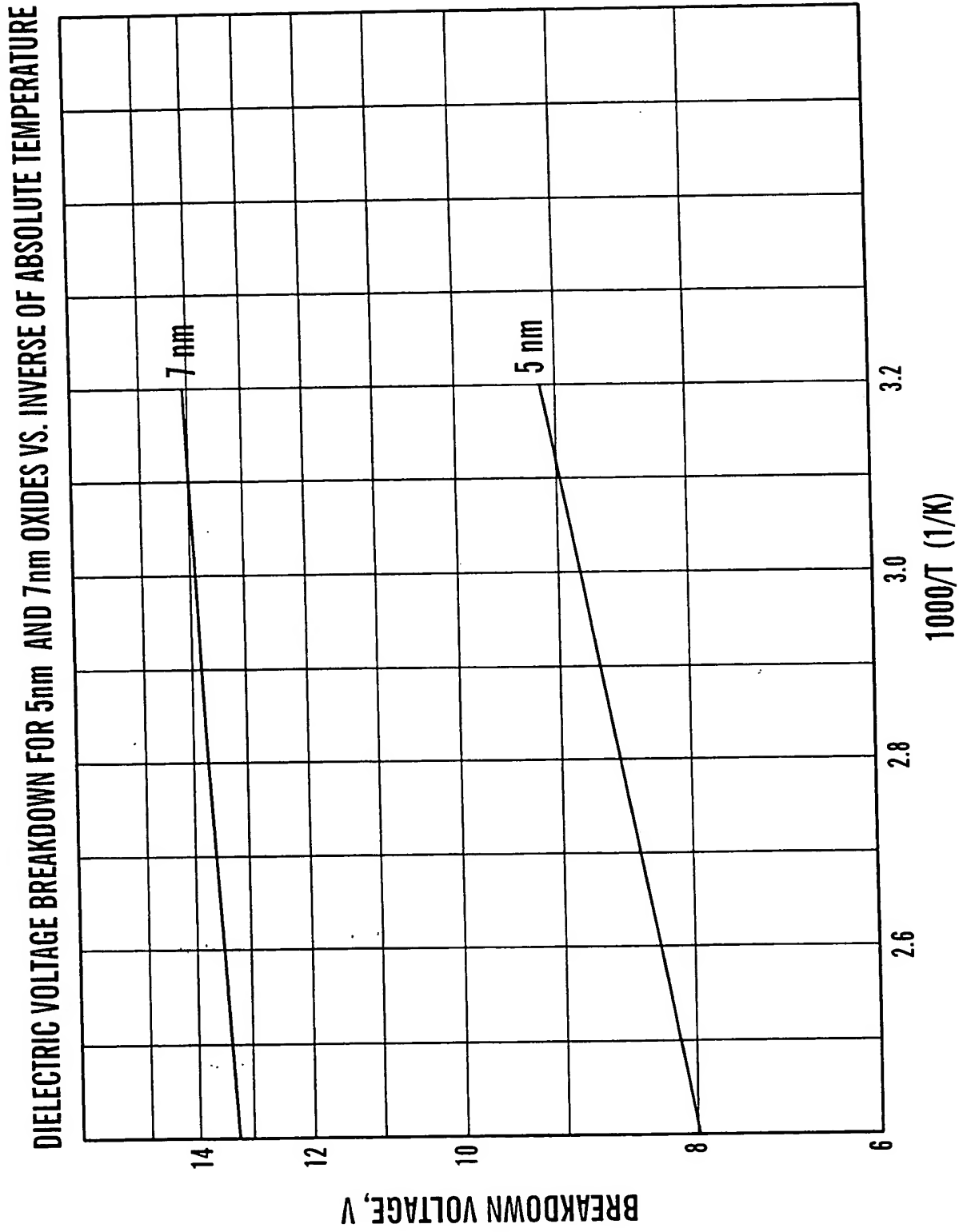


FIG. 18

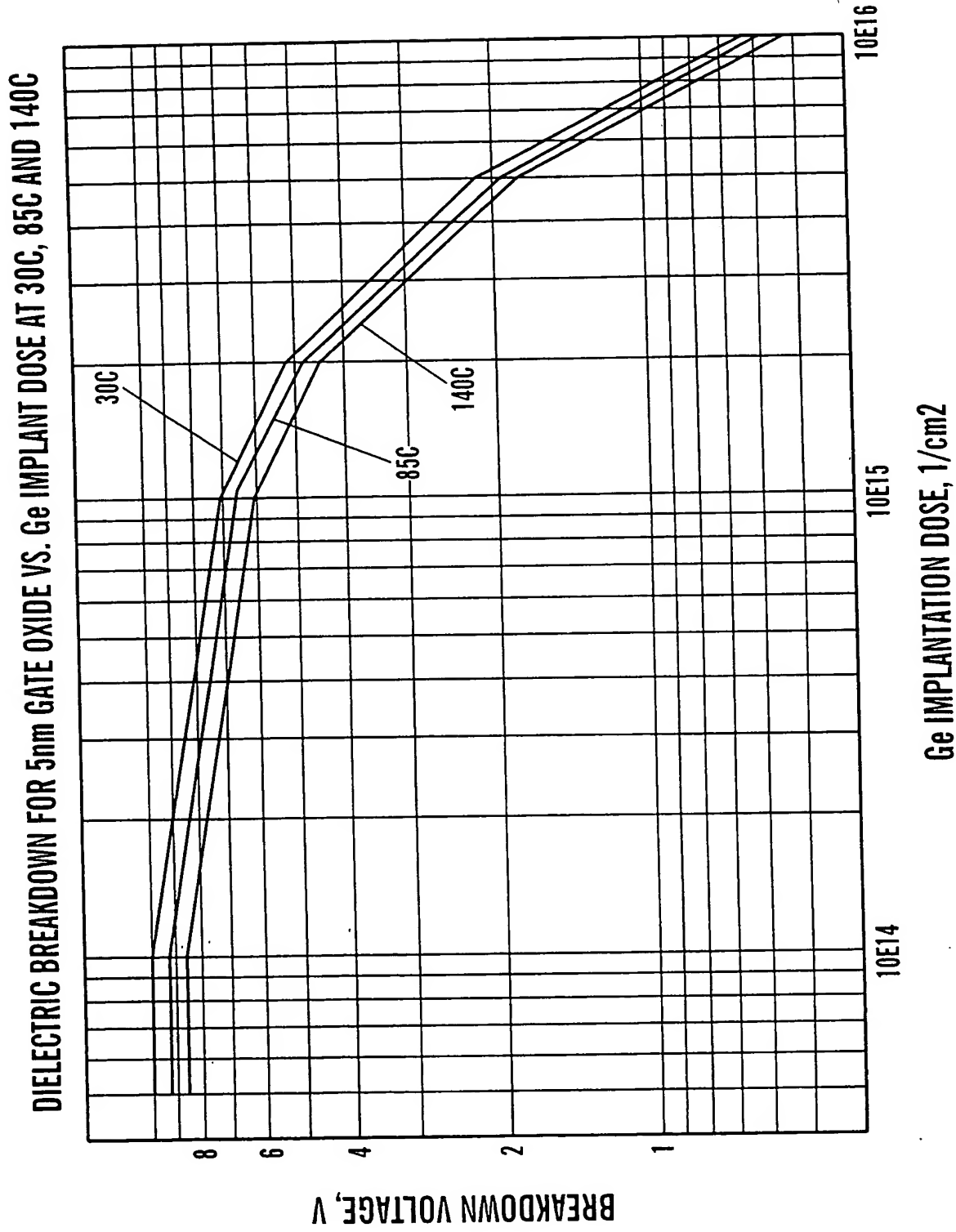


FIG. 19